

Integrated Privacy

Toggle and Brightness Control

System Architecture

Hewlett-Packard Confidential

Version 3.01

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**Revision History**

| **Revised By** | **Revision Number** | **Revision Date** | **Revision Description** |
| --- | --- | --- | --- |
| Thong Thai | 0.1 | 9/16/15 | Initial pre-Draft |
| Thong Thai | 0.2 | 1/22/16 | Draft |
| Thong Thai | 0.3 | 1/28/16 | Draft 2 |
| Thong Thai | 0.4 | 1/29/16 | Minor correction and clarification, add limitation, add “zero” brightness requirement |
| Thong Thai | 0.5 | 1/29/16 | Update persistence as a requirement. Add “smooth brightness”. Remove “zero” brightness requirement. |
| Thong Thai | 0.6 | 2/02/16 | Update architectural diagram, limitation. Add “zero” brightness back as a requirement. |
| Thong Thai | 0.61 | 2/15/16 | Add brightness slider diagram (3.1.1.1) for informational purposes |
| Thong Thai | 0.9 | 4/5/16 | * Change method of privacy adjustment (fn+f5/f6, fn+x) * Remove “zero” brightness requirement * Add 2-sec lid open delay requirement * Change “smooth brightness” from requirement to optional * Add typematic requirement for privacy adjustment |
| Thong Thai | 0.91 | 4/7/16 | * Set default Privacy level to “step 4” of privacy table * Clarify fn+p enable privacy if not already enable and set to “step 0” brightness (max privacy) |
| Thong Thai | 0.95 | 5/27/16 | * Add toaster/pop-up behavior and requirements along with associated WMI events and commands (3.2.1.3, 4.2.1, 4.2.2) |
| Thong Thai | 0.96 | 6/02/16 | * Slight update to toaster/pop-up behavior and requirements (3.2.1.3, 4.2.1) |
| Thong Thai | 1.01 | 1/26/17 | * Updated for Privacy Panel Gen 2 (2017) |
| Thong Thai | 1.02 | 3/28/17 | * Add “Force Enable HP Sure View” public WMI |
| Thong Thai | 1.03 | 6/28/17 | * Add EDID and sample brightness tables for Eastwood and Brando privacy panel |
| Thong Thai | 3.00 | 7/5/2018 | * Add Privacy Panel Gen 3 |
| Thong Thai | 3.01 | 8/28/2018 | * Fn+P removed for 2019 and onward * Add 2019 EC PWM by-pass (6.1.3) * Add EC/BIOS EDID requirement (4.6) * Update EC requirements for Gen3 (4.3.3) to include Panel ID detection |

Table 1 - History

# Overview

This document describes requirement and functionality of Integrated Panel Privacy feature.

# Requirements

## Supported Operating System

* Microsoft Windows 7, 8.1, 10 (Gen1)
* Microsoft Windows 10 (Gen2)
* All OS (limited supported – Gen 2, Gen 3)
  + TBD

# Functional behaviors

## Control and functionality

### General Control requirements

* Default mode is with Privacy turned off OOB.
* Privacy state will persist over Sx state. If power to EC is lost (force power reset for example), the system will boot with default state of Privacy off.

#### 2015 OOC requirements (Gen1)

* User toggles Privacy mode on/off via fn+f2 key.
* The default OOB privacy level is **2.**
* While Privacy mode is on
  + User may adjust privacy level / brightness using brightness hotkey (fn+f5/f6).
  + Press and hold fn+f5/f6 will repeat brightness adjustment.
  + OS brightness adjustments and features are NOT supported.
  + fn+p will set to privacy level 0.
* While Privacy mode is off
  + OS brightness adjustments and features are supported.
  + fn+p enable privacy at level 0.
* Persistence
  + The last brightness level for Privacy mode is persisted.
  + OS brightness adjustment may be made while Privacy mode is on, but does not take effect until Privacy mode is switched off.
* Brightness range
  + There are 6 privacy levels with level 0 being the most private / lowest brightness and level 5 being the least private / highest brightness.
  + The brightness range and individual brightness level are not the same between Privacy on/off modes. For examples:
    - Lowest level brightness in Privacy mode MAYBE dimmer than 0% brightness in non-Privacy mode.
    - Highest level brightness in Privacy mode MAYBE dimmer than 100% brightness in non-Privacy mode.
  + Range of brightness in Privacy mode MAYBE from 10nits to 80nits
  + Range of brightness in non-Privacy mode MAYBE from 15nits to 250nits.
* Brightness transition smoothly as user increase or decreases brightness.
* Brightness should transition from one level to the next level within 500ms in both Privacy modes and when switching between Privacy On and Off mode.

#### Gen 2 requirements (2017)

Same as 2015 OOC requirements above, with the following changes:

* Brightness range
  + There are **11** privacy levels with level 0 being the lowest level of panel’s brightness and level 10 being the highest level of panel’s brightness.
  + The brightness range and individual brightness level are not the same between Privacy and Sharing modes.
  + Range of brightness in Privacy mode should be close to the range of brightness in Sharing mode, but may not be exact.
  + Range of brightness in both modes are expected to be around 15 nits to 300 nits.
    - Update: Newer gen 2 panel (TBD) support up to 700 nits

#### Gen 3 requirements (2018)

Same as Gen 2, with the following changes:

* Brightness range
  + Range of brightness in Privacy mode is expected to be from ~5 nits to ~150 nits
  + Range of brightness in Sharing mode is expected to be from ~5 nits up to ~1000 nits (upper limit depends on each platform panel’s choice; 850nit might be a common upper limit after consideration of film and touch layers).

## Notification

#### General requirements

* TBD

#### 2015 OOC (Caesars)

* The LED on the Fn+F2 key is on when Privacy is enable.
* The LED on the Fn+F2 key is off when Privacy is disable.

#### 2015 OOC (Bellagio)

Toaster and slider pop-up is introduced with Bellagio OOC with the following behaviors:

Events:

* Boot and resume - No toaster or slider pop-up
* Fn+F2 (privacy mode toggle) key press
  + HP App will display toaster message with privacy on / off icon
* Fn+F5/F6 (privacy level) key press
  + While in Privacy enabled mode
    - HP App will display slider pop-up matching privacy level
    - ~~HP App will also display “Privacy” toaster~~
  + While in Privacy disabled mode
    - HP App will NOT display slider pop-up. Instead, brightness slider will be displayed by OS.
* Fn+P (maximum privacy) key press
  + HP App will display maximum privacy icon (full checkerboard icon). No slider pop-up.

Note that the pop-up slider is not interactive.

Please reference HP Hotkey Specification on GUI specifics.

#### Gen 2 requirements (2017)

Same as 2015 OOC (Bellagio) above

## Known Limitation

### General Limitation

#### 2015 OOC specific limitation

* Range of brightness in Privacy on mode is much less than range of brightness in Privacy off mode.
* Although Privacy should be functional in PreOS, it is not supported.
* OS brightness adjustments and features are not supported while Privacy mode is on.

#### Gen 2 limitation (2017)

* OS brightness adjustments and features are not supported while Privacy mode is on.

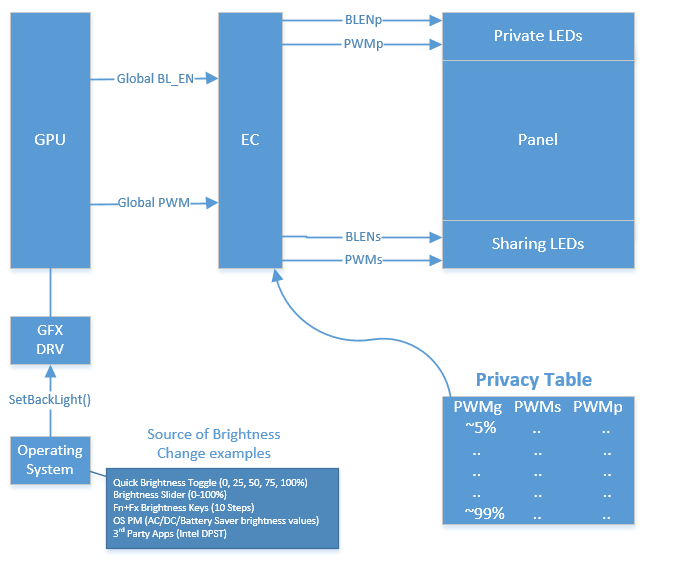
#### Gen 3 limitation (2018)

* Range of brightness in Privacy on mode is much less than range of brightness in Privacy off mode.
* OS brightness adjustments and features (such as OS’s automatic panel brightness) are not supported while Privacy mode is on.
* TBD: OS’s smooth brightness might not be achievable for Sharing mode.
  + Require testing with actual panel to determine.
  + May need MS waiver.

# Architecture and EC, BIOS Requirements

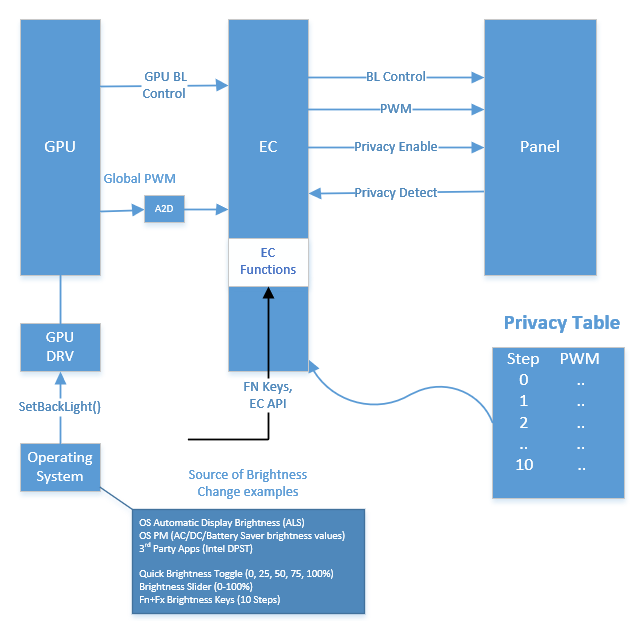
## Architecture

### Gen1 Architecture



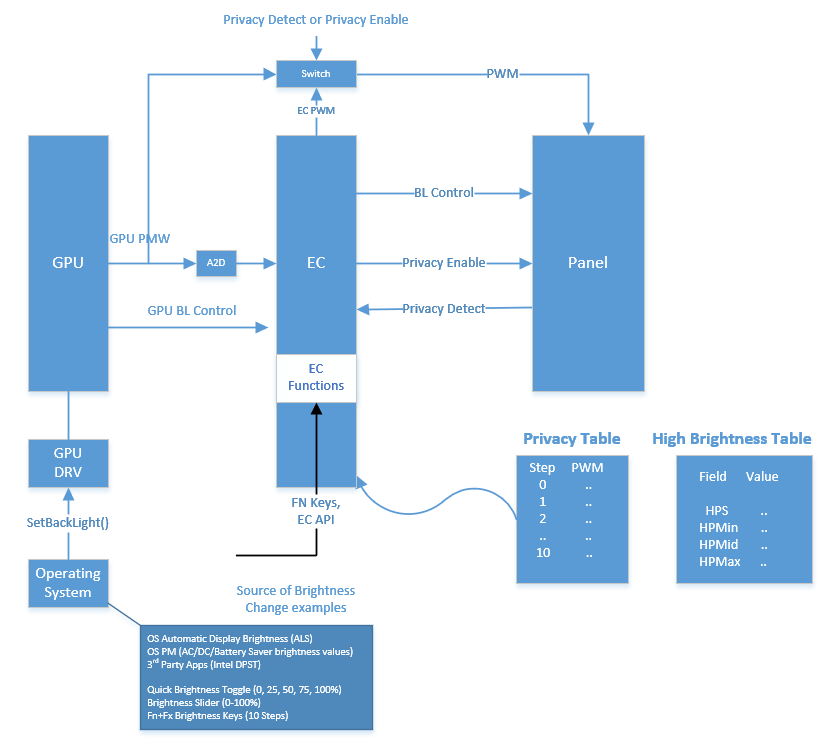
* Private LEDs – Backlight for privacy mode.
* Sharing LEDs – Backlight for standard/share mode and optionally for privacy mode
* Privacy Table – Global PWM to Private and Sharing PWM mapping table(s)
* Global PWM – PWM output from GPU which matches the OS’s brightness level
* Global BL\_EN – Backlight Enable control from GPU
* PWMp - PWM signal to drive the Privacy LEDs bank brightness level
* BLENp – Backlight Enable control for the Privacy LEDs bank
* PWMs – PWM signal to drive the Sharing LEDs bank brightness level
* BLENs – Backlight Enable control for the Sharing LEDs bank

### Gen2 Architecture



* Privacy Table – Privacy PWM table for Privacy mode
* Global PWM – PWM output from GPU which matches the OS’s brightness level
* BL\_EN – Backlight Enable control from GPU
* A2D – PWM to DC level R/C circuitry
* PWM - PWM signal to panel’s backlight
* Privacy Detect (PP\_Detect#) – signal to indicate if panel is a privacy panel
* Privacy Enable (PP\_HVA) – Privacy Enable / Disable control from EC to Panel

### Gen3 Architecture



* Privacy Table – Privacy PWM table for Privacy mode
* Source / Global PWM – PWM output from GPU which matches the OS’s brightness level
* BL\_EN – Backlight Enable control from GPU
* A2D – PWM to DC level R/C circuitry
* Destination PWM / PWM - PWM signal to panel’s backlight
* Privacy Panel Detect (PP\_Detect#) – signal to indicate if panel is a privacy panel
* Privacy Enable (PDLC) – Dual function signal
  + Privacy Enable / Disable control from EC to Panel (for Privacy mode)
  + Hight Brightness Enable / Disable control from EC to Panel (for Sharing mode)
* High Brightness Table
  + HPS – The Global PWM % value for EC to switch into high-brightness mode
  + HPMin – minimum PWM % value for high-brightness mode
  + HPMid – middle PWM % value for high-brightness mode
  + HPMax – max PWM % value for high-brightness mode
* Switch – select between GPU PWM or EC PWM
  + Controllable via either Privacy Detect or Privacy Enable signal. Used to by-pass EC PWM manipulation.

## 

Figure - Gen 3 High Brightness Mode vs Normal Brightness Mode

## Privacy Table

### Privacy Table for Gen1

* The privacy tables contain the information for EC to determine:
  + Which backlight (Private or Sharing or both) to enable in privacy on and privacy off mode.
  + Mapping of Global PWM % to Private PWM %, Sharing PWM %, or both in privacy on and privacy off mode.
  + Note: Global PWM values must be the same for both Privacy Off and Privacy On.
* The format of the table is below:

**Privacy Off:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| (Reference ONLY) Step # | Global PWM (from GPU) | PWM\_Sh  (Share LED Bank) | PWM\_Pr  (Private LED Bank) | BL\_Enable |
| 0 | Fill in values (5-100%) | Fill in values (5-100%) | Fill in values (5-100%) | Fill in values:  0-      All BL off  1-      Share BL on, Private BL off  2-      Share BL off, Private BL on  3-      Share BL on, Private BL on |
| 1 | .. | .. | .. | .. |
| 2 | .. | .. | .. | .. |
| 3 | .. | .. | .. | .. |
| 4 | .. | .. | .. | .. |
| 5 | .. | .. | .. | .. |
| 6 | .. | .. | .. | .. |
| 7 | .. | .. | .. | .. |
| 8 | .. | .. | .. | .. |
| 9 | .. | .. | .. | .. |
| 10 | .. | .. | .. | .. |

**Privacy On:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| (Reference ONLY) Step # | Global PWM (from GPU) | PWM\_Sh  (Share LED Bank) | PWM\_Pr  (Private LED Bank) | BL\_Enable |
| 0 | Fill in values (5-100%) | Fill in values (5-100%) | Fill in values (5-100%) | Fill in values:  0-      All BL off  1-      Share BL on, Private BL off  2-      Share BL off, Private BL on  3-      Share BL on, Private BL on |
| 1 | .. | .. | .. | .. |
| 2 | .. | .. | .. | .. |
| 3 | .. | .. | .. | .. |
| 4 | .. | .. | .. | .. |
| 5 | .. | .. | .. | .. |
| 6 | .. | .. | .. | .. |
| 7 | .. | .. | .. | .. |
| 8 | .. | .. | .. | .. |
| 9 | .. | .. | .. | .. |
| 10 | .. | .. | .. | .. |

### Privacy Table for Gen2 (2017)

* The privacy table for Gen 2 contain 11 PWM values corresponding to the 11 brightness steps.
* The final values will be determined by execution team.
* Sharing mode does not require a privacy table for Gen 2. In this mode, EC will “pass-through” PWM from GPU to the panel.

**Privacy Table (Gen2):**

|  |  |
| --- | --- |
| (Reference ONLY) Step # | PWM |
| 0 | Fill in values (5-100%) |
| 1 | .. |
| 2 | .. |
| 3 | .. |
| 4 | .. |
| 5 | .. |
| 6 | .. |
| 7 | .. |
| 8 | .. |
| 9 | .. |
| 10 | .. |

#### Privacy Table for Gen2 Automation (2017)

* The privacy table for Gen 2 may be automated starting with HP EDID 3.2. This updated EDID structure contain a 3 points PWM to Nits mapping (min, 60 nits, max) values for Privacy mode that BIOS and EC may use to auto-generate the 11 PWM values corresponding to the 11 brightness steps for privacy mode.
  + NOTE: This has been implemented via BCR 208185

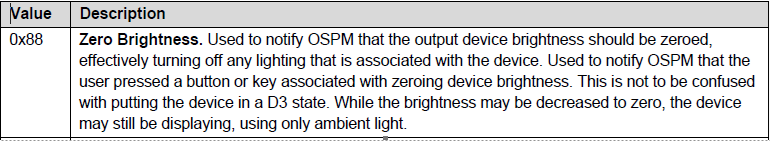
### Privacy Table for Gen3 (2018)

* Privacy mode will follow Gen2 implementation
* Sharing mode will follow a new implementation based on a set of “high brightness” values. These values are defined as follow to provide the following information
  + High Brightness PWM Switch (HBS) - The Global PWM % value for EC to switch into high-brightness mode
  + High Brightness PWM Min (HBMin) - The minimum % PWM value for high-brightness mode
  + High Brightness PWM Med (HBMid) - The middle % PWM value for high-brightness mode
  + High Brightness PWM Max (HBMax) - The maximum % PWM value for high-brightness mode
  + NOTE
    - Nits @ HBMin must be => Nits @ HBS
    - Nits @ HBMax => Nits @ HBMid => Nits @ HBMin
* Phase 1
  + In Phase 1, the above information is provided by the panel vendor and EC will hard-code them into internal table
* Phase 2
  + In Phase 2, the above information is provided by the panel vendor via Panel’s EDID, and EC will use the EDID values to create the internal table. EDID definition is TBD.

## EC requirements

### EC requirements for Gen 1

* EC will translate source PWM (Global PWM from GPU) to destination PWMs (PWMp & PWMs) based on active privacy state (off or on) and privacy table.
* As privacy table provide only 11 discrete steps values while Windows support up to 101 level of brightness, EC will perform piecewise linear interpolation for all missing values in between the 11 discrete steps.
* When Global BL\_EN is “off”, EC will not perform any PWM translation (PWMs output from EC is meaningless and maybe at any level).
* When Global BL\_EN is “on” EC will always perform PWM translation.
* EC will delay lid open notification to BIOS for 1.5 seconds. This delay is to mask the “wet out” artifact.
* When Privacy is ON
  + EC ignore global PWM from GPU
  + EC set PWMs (PWMp & PWMs) based on Privacy On Table
  + EC initial default is “Step 4” of the Privacy On Table
  + fn+p will set to “Step 0” of the Privacy On Table
  + fn+f6 will increase brightness by 2 steps (0>2>4>6>8>10>stop)
  + fn+f5 will decrease brightness by 2 steps (10>8>6>4>2>0>stop)
  + EC will support typematic feature for fn+f5/f6
  + EC will save and restore the last step (persistence) when switching Privacy On
* When Privacy is OFF
  + EC translate source PWM (Global PWM from GPU) to destination PWMs (PWMp & PWMs) based on Privacy Off Table
  + fn+p enable Privacy and set to “Step 0” of the Privacy On Table
* Optional: Smooth brightness: EC will adjust PWM\_Sh and PWM\_Pr in increment of 1% at 5ms interval.
* ~~When Privacy is enable, issue an ACPI notification to the panel device to set it to ZERO brightness.~~

~~~~

### EC requirements for Gen 2

* When Privacy is ON
  + EC ignore global PWM from GPU
  + EC set PWM based on Privacy Table
  + EC initial default is “Step 2” of the Privacy Table
  + fn+p will set to “Step 0” of the Privacy Table
    - 8/28/18- removed for Gen3 and all 2019 platforms (including Gen2)
  + fn+f6 will increase brightness by 1 step (0>1>2>..10>stop)
  + fn+f5 will decrease brightness by 1 step (10>9>8>..>0>stop)
  + EC will support typematic feature for fn+f5/f6
  + EC will save and restore the last step (persistence) when switching Privacy On
* When Privacy is OFF
  + EC pass-through the source PWM (Global PWM from GPU) to destination PWM.
    - NOTE: Due to ADC, reference voltage must be set correctly
  + fn+p enable Privacy and set to “Step 0” of the Privacy Table

### EC requirements for Gen 3

* Detecting Privacy Gen3
  + 2019 800’s series has a mixture of Gen2 and Gen3 panels. EC will read the Panel ID (see 4.6) to determine Privacy Panel generation. A table of Gen3 Panel IDs will be provided to EC.
    - EC will default to Gen2 behavior until it is able to obtain the Panel ID from BIOS to determine the generation.
* When Privacy is ON (same as Gen2)
  + EC ignore global PWM from GPU
  + EC set PWM based on Privacy Table
  + EC initial default is “Step 2” of the Privacy Table
  + ~~fn+p will set to “Step 0” of the Privacy Table~~
    - ~~CONFLICT with existing fn+p. When NumLk is on, fn+p should be “P”, but is not because of this requirement. Discussion with ST to resolve is in progress.~~
    - 8/28/18- removed for Gen3 and all 2019 platforms (including Gen2)
  + fn+f6 will increase brightness by 1 step (0>1>2>..10>stop)
  + fn+f5 will decrease brightness by 1 step (10>9>8>..>0>stop)
  + EC will support typematic feature for fn+f5/f6
  + EC will save and restore the last step (persistence) when switching Privacy On
* When Privacy is OFF (new for Gen3)
  + EC pass-through the source PWM (Global PWM from GPU) to destination PWM for Global PWM values up to High Brightness PWM Switch
    - NOTE: Due to ADC, reference voltage must be set correctly
  + Phase 1
    - High Brightness values:
      * HBS is hardcoded to 90% (vendor may change)
      * HBMin will be provided by the panel vendor
      * HBMid is not used
      * HBMax is hardcoded to 100%
    - When source PWM is less than HBS, EC pass-through the source PWM to destination PWM
    - When source PWM is equate to or greater than HBS, EC map source PWM to destination PWM using the following equation:
      * **Destination PWM = HBMin + (Source PWM – HBS)\*(HBMax-HBMin) /(100-HBPS)**
      * E.g. with HBS=90, HBMax=100
        + Destination PWM = HBMin + (Source PWM – 90)\*(100-HPMin) / 10
    - Hysteresis is required to avoid constant changes between high brightness and normal brightness mode when the user has the brightness slider set to the HBS or HBS+/-1 value
      * i.e. if HBS = 90%, EC may transition to high brightness or normal brightness when the user transition to 89, 90 or 91 % brightness slider position. Once the transition has occurred, no transition shall occur while the brightness slider position remains unchanged.
  + Phase 2
    - High Brightness values are not hardcoded, and is provided through panel’s EDID (TBD)
    - When source PWM is less than HBS, EC pass-through the source PWM to destination PWM
    - When source PWM is equate to or greater than HBS, EC map source PWM to destination PWM using the following equation:
      * If HBMid is < HBMin or > HBMax (HBMid is not used)
        + **Destination PWM = HBMin + (Source PWM – HBS)\*(HBMax-HBMin) /(100-HBPS)**
      * Else (HBMid is used)
        + **TBD**
    - Hysteresis is required to avoid constant changes between high brightness and normal brightness mode when the user has the brightness slider set to the HBS or HBS+/-1 value
      * i.e. if HBS = 90%, EC may transition to high brightness or normal brightness when the user transition to 89, 90 or 91 % brightness slider position. Once the transition has occurred, no transition shall occur while the brightness slider position remains unchanged.
  + NOTE: High Brightness PWM definition
    - High Brightness PWM Switch (HBS) - The Global PWM % value for EC to switch into high-brightness mode
    - High Brightness PWM Min (HBMin) - The minimum % PWM value for high-brightness mode
    - High Brightness PWM Med (HBMid) - The middle % PWM value for high-brightness mode
    - High Brightness PWM Max (HBMax) - The maximum % PWM value for high-brightness mode

## 

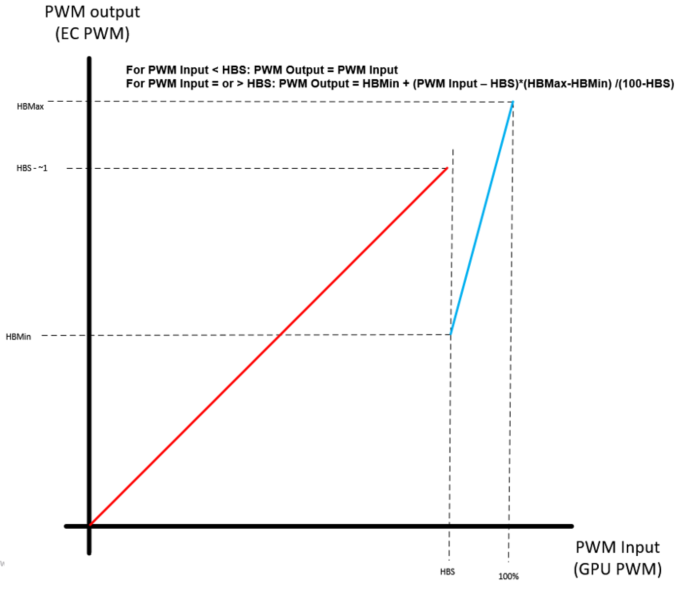


Figure PWM Input to PWM Output for Sharing Mode (Gen 3- Phase 1)

## EC and BIOS Requirement to support toaster and slider pop-up.

Toaster and slider pop-up is introduced with Bellagio OOC with the following behaviors and requirements:

Events:

* Boot and resume - No toaster or slider pop-up
* Fn+F2 (privacy mode toggle) key press
  + **BIOS send ‘Privacy Panel Event’ with Privacy State (On or Off)**
  + HP App will display toaster message with privacy on / off icon
* Fn+F5/F6 (privacy level) key press
  + While in Privacy enabled mode
    - **BIOS send ‘Privacy Panel Event’ with updated Visibility Percent (0 to 100d)**
    - HP App will display slider pop-up matching privacy level
    - ~~HP App will also display “Privacy” toaster~~
  + While in Privacy disabled mode
    - HP App will NOT display slider pop-up. Instead, brightness slider will be displayed by OS.
* Fn+P (maximum privacy) key press
  + **BIOS send ‘Privacy Panel Event’ with Privacy State = ‘Enter Max Privacy’**
  + HP App will display maximum privacy icon (full checkerboard icon). No slider pop-up.

Note that the pop-up slider is not interactive.

Please reference HP Hotkey Specification on GUI specifics.

## WMI for Privacy Panel

### Private WMI Event and Commands for Privacy Panel

Please reference BIOS WMI Specification for current version.

|  |  |  |
| --- | --- | --- |
| **Event ID** | **Description** | **Event Data** |
| 14h | Privacy Panel Event | Byte 0: Privacy Panel State  FFh = Privacy Mode is Off  FEh = Privacy Mode is On  FDh = Enter Max Privacy  00h = No change to mode  Byte 1: Visibility Percentage  0-100d  Bytes 2-3: Reserved  Notes:   * 0% is the most private. * Only available on systems with a Privacy Panel |

| **Command type** | **Input data size**  **(bytes)** | **Return data size**  **(bytes)** | **Data buffer** |
| --- | --- | --- | --- |
| 3Eh | 4 | 0 | **Set Privacy Panel State**  On input:  Byte 0: Privacy Panel State  FFh = Privacy Mode is Off  FEh = Privacy Mode is On  FDh = Enter Max Privacy  FCh = Force enable Privacy Mode  FBh = Exit force enable Privacy Mode  FAh = Reserved  00h = No change to mode  Byte 1: Privacy Adjustment  FFh = Increase percentage  FEh = Decrease percentage  00h = No adjustment  Bytes 2-3: Reserved  Notes:   * Any changes caused by this command will generate a Privacy Panel Event * The lower the percentage, the more private. * Max Private is defined as entering privacy mode at the lowest level.  It is a jump to the maximum amount of privacy. * Privacy Adjustment can be set simultaneously with Privacy Panel State if turning on Privacy Mode or entering Max Privacy. * Privacy Adjustment is ignored while Privacy Mode is off. * Only available on systems with a Privacy Panel * Force enable Privacy Mode turns on Privacy Mode and does not let the user disable it with the hotkey * From Force enable Privacy Mode, send Exit before attempting to turn Privacy Mode Off |
| 3Eh | 0 | 4 | **Get Privacy Panel State**  On output:  Byte 0: Privacy Panel State  FFh = Privacy Mode is Off  FEh = Privacy Mode is On  FDh = Reserved  FCh = Force enable Privacy Mode  FBh = Reserved  FAh = Privacy Panel unsupported  Byte 1: Visibility Percentage  0-100d  Bytes 2-3: Reserved  Refer to the notes in the Set command. |

### Public WMI for Privacy Panel

#### Force Enable HP Sure View option (BCR 198132)

“Force enable HP Sure View” in F10 option with the following definition:

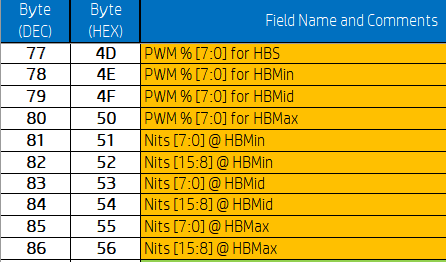
* “Enable”
  + HP Sure View is enabled, F2 cannot be used to disable Sure View
* “Disable” (default)
  + HP Sure View is not force enabled, F2 can be used to toggle Sure View state

When switching from “Enable” to “Disable”, Sure View will be switched into Sharing mode.

## EC and BIOS Requirement for Panel’s EDID

BIOS will read Panel’s EDID data and pass the data to EC through ECRAM (to be defined by developer).

The data to be passed on are:

* Panel ID
  + UINT16  ManufactureName;                                 // (0x08) Manufacturer ID
  + UINT16  ProductCode;                                            // (0x0A) Product ID Code
* High Brightness Table
  + Draft version of table in EDID
  + 

### HP EDID Format for reference

//

// HP EDID Format Version 3.2 (VESA EDID 1.4)

//

typedef struct {

  UINT8   Header[8];                                                  // (0x00) EDID header "00 FF FF FF FF FF FF 00"

  UINT16  ManufactureName;                                 // (0x08) Manufacturer ID

  UINT16  ProductCode;                                            // (0x0A) Product ID Code

  UINT32  SerialNumber;                                          // (0x0C) 32-bit serial number

  UINT8   WeekOfManufacture;                             // (0x10) Week of manufacture

  UINT8   YearOfManufacture;                                // (0x11) Year of manufacture

  UINT8   EdidVersion;                                              // (0x12) EDID Structure Version

  UINT8   EdidRevision;                                             // (0x13) EDID Structure Revision

  UINT8   VideoInputDefinition;                              // (0x14) Video input definition

  UINT8   MaxHorizontalImageSize;                        // (0x15) Maximum H image size

  UINT8   MaxVerticalImageSize;                             // (0x16) Maximum V image size

  UINT8   DisplayTransferCharacteristic;                 // (0x17) Display Gamma

  UINT8   FeatureSupport;                                          // (0x18) Feature support

  UINT8   RedGreenLowBits;                                       // (0x19) Red/green low bits

  UINT8   BlueWhiteLowBits;                                      // (0x1A) Blue/white low bits

  UINT8   RedX;                                                             // (0x1B) Red x/ high bits

  UINT8   RedY;                                                            // (0x1C) Red y

  UINT8   GreenX;                                                        // (0x1D) Green x

  UINT8   GreenY;                                                        // (0x1E) Green y

  UINT8   BlueX;                                                           // (0x1F) Blue x

  UINT8   BlueY;                                                           // (0x20) Blue y

  UINT8   WhiteX;                                                        // (0x21) White x

  UINT8   WhiteY;                                                         // (0x22) White y

  UINT8   EstablishedTimings[3];                              // (0x23) Established timing 1, 2, 3

  UINT8   StandardTimingIdentification[16];         // (0x26) Standard timing #1, #2, #3, #4, #5, #6, #7, #8

//----------------------------------------------------------------------------------------------------

  UINT8   DetailedTimingDescriptions1[18];          // (0x36) Detail timing/monitor descriptor #1

//----------------------------------------------------------------------------------------------------

  UINT8   DetailedTimingDescriptions2[18];           // (0x48) Detail timing/monitor descriptor #2

//----------------------------------------------------------------------------------------------------

  UINT8   DetailedTimingDescriptions3;                  // (0x5A) Detail timing/monitor descriptor #3

  UINT8   Flag30;                                                          // (0x5B)

  UINT8   Reserved3;                                                   // (0x5C)

  UINT8   BrightnessTablePrivacyModeHeader;    // (0x5D) For Brightness Table and Power Consumption v2 2nd Table (Optional - Privacy Mode)

                                                                                       //         0x03: support both normal and high nit panel

  UINT8   Flag31;                                                          // (0x5E)

  UINT8   PrivacyModePWM0;                                  // (0x5F) PWM % [7:0] @ Step 0

  UINT8   PrivacyModePWM5;                                  // (0x60) PWM % [7:0] @ Step 5

  UINT8   PrivacyModePWM10;                               // (0x61) PWM % [7:0] @ Step 10

  UINT8   PrivacyModeNits0;                                    // (0x62) Nits [7:0] @ Step 0

  UINT8   PrivacyModeNits5;                                    // (0x63) Nits [7:0] @ Step 5

  UINT8   PrivacyModeNits10\_L;                             // (0x64) Nits [7:0] @ Step 10 = (0x0001 = 2 nits, 0x00FF = 510 nits, 0x09C4 = 5000 nits)

  UINT8   PowerConsumption3[3];                        // (0x65) Panel Electronics Power @ 32x32 Chess Pattern =

                                                                                     // (0x66) Backlight Power @ 60 nits =

                                                                                     // (0x67) Backlight Power @ Step 10 =

  UINT8   PrivacyModeMaxNits\_L;                         // (0x68) Nits [7:0] @ 100% PWM Duty = (0x0001 = 2 nits, 0x00FF = 510 nits, 0x09C4 = 5000 nits)

  UINT8   PrivacyModeNits10\_H;                            // (0x69) Nits [15:8] @ Step 10 = (0x0001 = 2 nits, 0x00FF = 510 nits, 0x09C4 = 5000 nits)

  UINT8   PrivacyModeMaxNits\_H;                        // (0x6A) Nits [15:8] @ 100% PWM Duty = (0x0001 = 2 nits, 0x00FF = 510 nits, 0x09C4 = 5000 nits)

  UINT8   Flag32;                                                        // (0x6B) Flag

//----------------------------------------------------------------------------------------------------

  UINT8   DetailedTimingDescriptions4;                 // (0x6C) Detail timing/monitor descriptor #4

  UINT8   Flag40;                                                         // (0x6D)

  UINT8   Reserved4;                                                 // (0x6E)

  UINT8   BrightnessTableSharingModeHeader; // (0x6F) For Brightness Table and Power Consumption v2 Primary Table (Sharing Mode)

                                                                                     //         0x02: Support normal nit panel only [up to 510nits], it follows HP EDID v3.1 spec.

                                                                                     //         0x03: Support both normal and high nit panel, it follows HP EDID v3.2 spec.

  UINT8   Flag41;                                                       // (0x70)

  UINT8   SharingModePWM0;                              // (0x71) PWM % [7:0] @ Step 0

  UINT8   SharingModePWM5;                              // (0x72) PWM % [7:0] @ Step 5

  UINT8   SharingModePWM10;                           // (0x73) PWM % [7:0] @ Step 10

  UINT8   SharingModeNits0;                                // (0x74) Nits [7:0] @ Step 0

  UINT8   SharingModeNits5;                                // (0x75) Nits [7:0] @ Step 5

  UINT8   SharingModeNits10\_L;                          // (0x76) Nits [7:0] @ Step 10 = (0x0001 = 2 nits, 0x00FF = 510 nits, 0x09C4 = 5000 nits)

  UINT8   PowerConsumption4[3];                       // (0x77) Panel Electronics Power @ 32x32 Chess Pattern =

                                                                                   // (0x78) Backlight Power @ 60 nits =

                                                                                   // (0x79) Backlight Power @ Step 10 =

  UINT8   SharingModeMaxNits\_L;                      // (0x7A) Nits [7:0] @ 100% PWM Duty = (0x0001 = 2 nits, 0x00FF = 510 nits, 0x09C4 = 5000 nits)

  UINT8   SharingModeNits10\_H;                        // (0x7B) Nits [15:8] @ Step 10 = (0x0001 = 2 nits, 0x00FF = 510 nits, 0x09C4 = 5000 nits)

  UINT8   SharingModeMaxNits\_H;                     // (0x7C) Nits [15:8] @ 100% PWM Duty = (0x0001 = 2 nits, 0x00FF = 510 nits, 0x09C4 = 5000 nits)

  UINT8   Flag42;                                                     // (0x7D) Flag

//----------------------------------------------------------------------------------------------------

  UINT8   ExtensionFlag;                                        // (0x7E) Number of (optional) 128-byte EDID extension blocks to follow

  UINT8   Checksum;                                              // (0x7F) Checksum

 UINT8   ExtensionBlocks[128];                          // (0x80)

} HP\_EDID\_FORMAT;

# Dependency

## Privacy Table

* ODM or Panel team must provide privacy tables
* Starting with Gen2, the privacy PWM table is auto-generated for Gen2 panel with Privacy Brightness table

## Brightness Tables in EDID

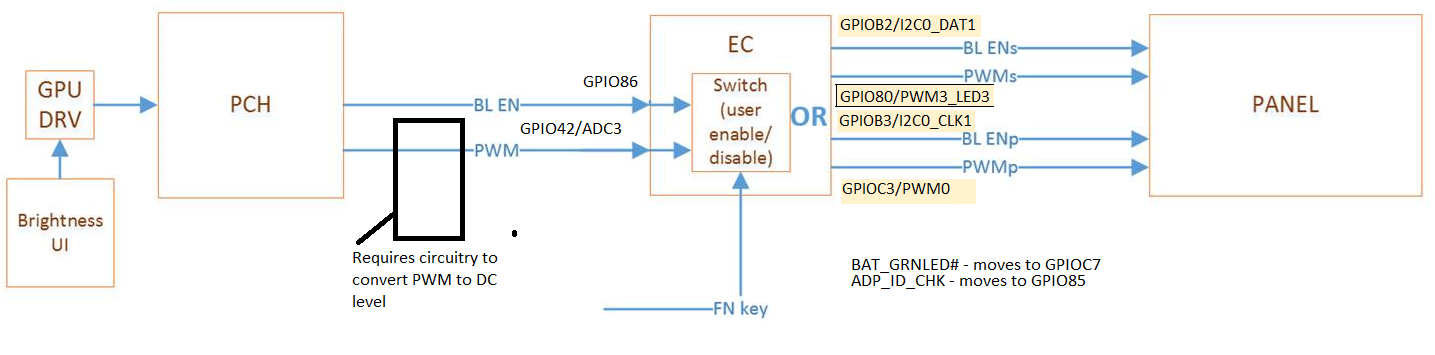
* The Brightness Table in EDID is still required as it is used as the “index” to map Global PWM to Share and Private PWM (Gen1)
* Gen 2 (and future Gen) Privacy Panel must include brightness table in panel’s EDID for both sharing mode and privacy mode (see HP EDID v3.2)
* Gen 3 Privacy Panel vendor must provide high brightness table that include HBS and HBMin value (Phase 1)
  + Panel vendor must define HBS and HBMin such that the transition from sharing’s normal brightness to high brightness and vice-versa is “smooth” and “proportional”
    - E.g. If HBS is 90% and 89% PWM (standard brightness) is 360 nits, PWM at HBMin should yield higher than 360 nits.
* Gen 3 Privacy Panel must include high brightness table in panel’s EDID that include HBS, HBMin, HBMid, HBMax (Phase 2). EDID definition TBD.

## Lowest Brightness level is NOT off

* The lowest brightness level, known as “Zero Brightness” in ACPI specification could be defined as actual off (no backlight brightness output) or as the lowest level of brightness supported. This level for Privacy feature must be set to the lowest brightness supported level and not to OFF.

# Hardware Interface (Reference)

### Hardware Interface for Caesars



|  |  |  |
| --- | --- | --- |
| Pin | Current Caesars | Privacy Caesars |
| GPIO42/ADC3 | WWAN\_DET# (Reserved, NI) | PWM\_IN(requires ext hardware) |
| GPIO80/PWM3\_LED3 | ADP\_ID\_CHK | PWM\_OUT1 (shared) |
| GPIO85/RXD | Not used | ADP\_ID\_CHK |
| GPIO86/TXD/SHD\_CS1# | Not used | BL\_EN\_IN |
| GPIOB2/I2C0\_DAT1 | Not used | BL\_EN\_OUT1(shared) |
| GPIOB3/I2C0\_CLK1 | Not used | BL\_EN\_OUT2 (private) |
| GPIOC3/PWM0 | BAT\_GRNLED# | PWM\_OUT2 (private) |
| GPIOC7 | Not used | BAT\_GRNLED# |
| GPIO42/ADC3 | WWAN\_DET# (Reserved, NI) | PWM\_IN(requires ext hardware) |
| GPIO80/PWM3\_LED3 | ADP\_ID\_CHK | PWM\_OUT1 (shared) |
| GPIO85/RXD | Not used | ADP\_ID\_CHK |
| GPIO86/TXD/SHD\_CS1# | Not used | BL\_EN\_IN |

### Hardware Interface for Gen2 (include Oldman as reference)

#### ADC and reference voltage

Due to PWM to DC converter, the proper ADC internal reference voltage is required.

The following show an actual ADC reading from EC on Oldman shipping configuration (200Hz PWM output from PCH/GPU). The ADC internal reference voltage is 2.67V.

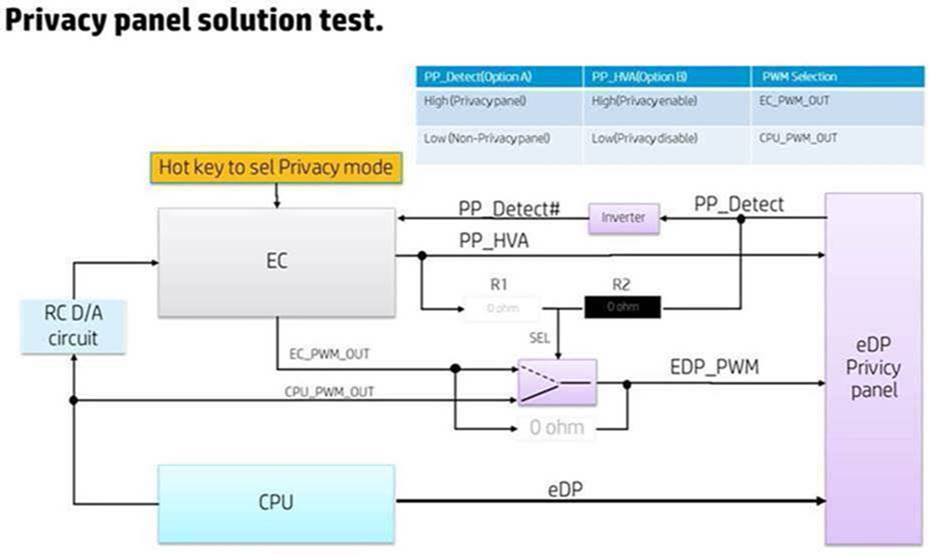
|  |  |  |
| --- | --- | --- |
| OS Brightness % | ADC (V)  EC reading | GPU/PCH PWM OUT% (INV\_PWM\_OUT) |
| 0 | 0.127 | 4.8 |
| 10 | 0.165 | 6.4 |
| 20 | 0.226 | 8.8 |
| 30 | 0.303 | 11.2 |
| 40 | 0.396 | 15.2 |
| 50 | 0.534 | 20 |
| 60 | 0.732 | 27.2 |
| 70 | 1.015 | 37.6 |
| 75 | 1.202 | 45.6 |
| 80 | 1.403 | 52.8 |
| 90 | 1.925 | 72 |
| 99 | 2.582 | 96.89 |
| 100 | 2.670 | 100 |

The following show an actual ADC reading from EC on Oldman with a 1KHz PWM output from PCH/GPU and a modified ADC (1KHz is targeted for next Gen in 2018). The ADC internal reference voltage is 2.813V.

|  |  |  |
| --- | --- | --- |
| OS Brightness % | ADC (V)  EC reading | GPU/PCH PWM OUT% (INV\_PWM\_OUT) |
| 0 | 0.121 | 4.8 |
| 10 | 0.165 | 6.4 |
| 20 | 0.242 | 8.8 |
| 30 | 0.314 | 11.2 |
| 40 | 0.407 | 15.2 |
| 50 | 0.558 | 20 |
| 60 | 0.773 | 27.2 |
| 70 | 1.075 | 37.6 |
| 75 | 1.271 | 45.6 |
| 80 | 1.488 | 52.8 |
| 90 | 2.030 | 72 |
| 99 | 2.747 | 96.89 |
| 100 | 2.813 | 100 |

### EC PWM by-pass for 2019 (Gen2 and Gen3)

Due to risk of not being able to meet Microsoft’s smooth brightness requirement for non-privacy and for sharing mode with privacy panel, EC PWM by-pass circuitry is added to all 2019 systems with privacy SKU. The PWM output to the panel should only go through EC when necessary.  When not necessary, it by-pass the EC and the output is straight from the GPU.   The circuitry to by-pass EC is HW based, using the PP\_Detect signal (from panel) for Option A.  For Option B, the PP\_HVA signal is driven by EC, which is asserted for Privacy mode and is not asserted for non-Privacy mode and for non-Privacy panel.

The decision on option A or B is to be determined later during execution of 2019 platform. If Option B is selected, EC must not assert PP\_HVA for non-privacy panel. For privacy panel, EC shall follow the requirements as outlined for Gen3 and Gen2 above.

# 

# Privacy Table example (Reference)

Note: Table is only an example. It is NOT accurate.

## Privacy Table example on Caesars

**Privacy Off:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| (Reference ONLY) Step # | Global PWM (from GPU) | PWM\_Sh  (Share LED Bank) | PWM\_Pr  (Private LED Bank) | BL\_Enable |
| 0 | 10 | 5 | 5 | 3 |
| 1 | 15 | 20 | 10 | 3 |
| 2 | 22 | 30 | 15 | 3 |
| 3 | 27 | 40 | 20 | 3 |
| 4 | 35 | 50 | 30 | 3 |
| 5 | 45 | 55 | 33 | 3 |
| 6 | 58 | 60 | 35 | 3 |
| 7 | 72 | 70 | 40 | 3 |
| 8 | 82 | 80 | 50 | 3 |
| 9 | 91 | 90 | 55 | 3 |
| 10 | 99 | 99 | 60 | 3 |

**Privacy On:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| (Reference ONLY) Step # | Global PWM (from GPU) | PWM\_Sh  (Share LED Bank) | PWM\_Pr  (Private LED Bank) | BL\_Enable |
| 0 | 10 |  | 5 | 2 |
| 1 | 15 |  | 10 | 2 |
| 2 | 22 |  | 14 | 2 |
| 3 | 27 |  | 19 | 2 |
| 4 | 35 |  | 25 | 2 |
| 5 | 45 |  | 30 | 2 |
| 6 | 58 |  | 35 | 2 |
| 7 | 72 |  | 39 | 2 |
| 8 | 82 |  | 44 | 2 |
| 9 | 91 |  | 49 | 2 |
| 10 | 99 |  | 50 | 2 |

## Privacy Table example on Oldman

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **OS Brightness %**  **(range: 0-100%)**  **Sharing** | **GPU/PCH**  **PWM Out %**    (INV\_PWM\_OUT)  **Sharing** | **PWM EC IN**  (not accurate due to probe)  **Sharing** | **PWM% EC OUT**  (official 1.02)    **WITHOUT**  **EC FIX**  **Sharing** | **PWM% EC OUT**  (after official 1.05)  Bootleg 1.02    **With EC FIX**  **Sharing** |  | **Brightness**  **Hotkey Steps**  **Privacy** | **PWM% EC OUT**  **(official 1.02)**  **Privacy** | **PWM% EC OUT**  **(after official 1.05)**  **Bootleg 1.02**  **Privacy** |
| 0 | 4.8 | 0.120 V | 4 | 5 |  | 0 | 1 | 1 |
| 10 | 6.4 | 0.152 | 6 | 6 |  | 1 | 10 | 6 |
| 20 | 8.8 | 0.200 | 8 | 8 |  | 2 | 20 | 8 |
| 30 | 11.2 | 0.268 | 11.2 | 11 |  | 3 | 30 | 11 |
| 40 | 15.2 | 0.348 | 14.2 | 15 |  | 4 | 40 | 15 |
| 50 | 20 | 0.472 V | 18.6 | 20 |  | 5 | 50 | 20 |
| 60 | 27.2 | 0.636 | 26 | 27 |  | 6 | 60 | 27 |
| 70 | 37.6 | 0.884 | 36 | 38 |  | 7 | 70 | 38 |
| 75 | 45.6 |  |  |  |  | n/a |  |  |
| 80 | 52.8 | 1.212 | 49 | 53 |  | 8 | 80 | 53 |
| 90 | 72 | 1.65 | 68 | 73 |  | 9 | 90 | 73 |
| 99 | 96.89 |  |  |  |  | n/a |  |  |
| 100 | 100 | 2.30V | 95 | 100 |  | 10 | 100 | 100 |

|  |  |  |  |
| --- | --- | --- | --- |
|  | **Brightness**  **Hotkey Steps**  **Privacy** | **PWM% EC OUT**  **(official 1.02)**  **Privacy** | **PWM% EC OUT**  **(after official 1.05)**  **Privacy** |
|  | 0 | 1 | 1 |
|  | 1 | 10 | 6 |
|  | 2 | 20 | 8 |
|  | 3 | 30 | 11 |
|  | 4 | 40 | 15 |
|  | 5 | 50 | 20 |
|  | 6 | 60 | 27 |
|  | 7 | 70 | 38 |
|  | 8 | 80 | 53 |
|  | 9 | 90 | 73 |
|  | 10 | 100 | 100 |

## Privacy Table example on Eastwood and Brando

For Eastwood (12.5)

|  |  |  |
| --- | --- | --- |
|  | **Brightness**  **Hotkey Steps**  **Privacy** | **PWM% EC OUT**  **Privacy** |
|  | 0 | 1.7% (~5 nits) |
|  | 1 | 6 |
|  | 2 | 8 |
|  | 3 | 11 |
|  | 4 | 15 |
|  | 5 | 20.2% (~57 nits) |
|  | 6 | 27 |
|  | 7 | 38 |
|  | 8 | 53 |
|  | 9 | 73 |
|  | 10 | 100% (~280 nits) |

For Brando (14, for both Touch and non-Touch)

|  |  |  |
| --- | --- | --- |
|  | **Brightness**  **Hotkey Steps**  **Privacy** | **PWM% EC OUT**  **Privacy** |
|  | 0 | 1.6% (~5 nits) |
|  | 1 | 6 |
|  | 2 | 8 |
|  | 3 | 11 |
|  | 4 | 15 |
|  | 5 | 19.1% (~57 nits) |
|  | 6 | 27 |
|  | 7 | 38 |
|  | 8 | 53 |
|  | 9 | 73 |
|  | 10 | 100% (~297 nits - Touch) |

# Panel EDID (Reference)

## For 12.5 and 14 (2017)

Privacy table:

* Step0= 5 nits
* Step5= 60 nits
* Step10 = 315 nits (14”) / 297 nits (12.5”)

Sharing table:

* Step0= 15 nits
* Step 5 = 60 nits
* Step 10 = 630 nits (14” & 12.5”)

**Time #3 & Time #4 :**

**Step 0/ brightness:  privacy/ 5nit,  sharing /15nit;**

**PWM include the 10% TP loss account**

|  |  |  |  |
| --- | --- | --- | --- |
| **Address** | **Field Name and Comments** | **M140NVF7 R0** | |
| **(Hex)** | **Simulation** | **Note(14")** |
| **700nits Ver.** |
| 5B | Flag | 00 |  |
| 5C | Reserved | 00 |  |
| 5D | For Brightness Table and Power cosumption v2 2nd Table(Optional - Privacy Mode) | 03 |  |
| 5E | Flag | 00 |  |
| 5F | PWM %[7:0] @ Step 0 | 04 | [1.6%@5.6nits(5nits+10%TP](mailto:1.6%25@5.6nits(5nits+10%25TP) loss) |
| 60 | PWM %[7:0] @ Step 5 | 30 | [19.1%@66.7nits(60nits+10%TP](mailto:19.1%25@66.7nits(60nits+10%25TP) loss) |
| 61 | PWM %[7:0] @ Step 10 | FF | 100%@350nits |
| 62 | Nits [7:0] @ Step 0 | 05 | 5nits |
| 63 | Nits [7:0] @ Step 5 | 3C | 60nits |
| 64 | Nits [7:0] @ Step 10 | 9D | 315nits(350nits-10%TP loss) |
| 65 | Panel Electronics Power @32\*32 Chess Pattern= | 2B | 1.74W |
| 66 | Backlight Power @60 nits= | 14 | 0.82W |
| 67 | Backlight Power @Step 10= | 39 | 4.57W |
| 68 | Nits [7:0] @ 100% PWM Duty= | 9D | 315nits(350nits-10%TP loss) |
| 69 | Nits [15:8] @ Step 10 | 00 | 315nits(350nits-10%TP loss)[15:8] |
| 6A | Nits [15:8] @ 100% PWM Duty= | 00 | 315nits(350nits-10%TP loss) [15:8] |
| 6B | Flags | 00 |  |
| 6C | Detailed Timing Description #4 | 00 |  |
| 6D | Flag | 00 |  |
| 6E | Reserved | 00 |  |
| 6F | For Brightness Table and Power cosumption v2 Primary Table(Sharing Mode) | 02 |  |
| 70 | Flag | 00 |  |
| 71 | PWM %[7:0] @ Step 0 | 06 | [2.4%@16.7nits(15nits+10%TP](mailto:2.4%25@16.7nits(15nits+10%25TP) loss) |
| 72 | PWM %[7:0] @ Step 5 | 18 | [9.5%@66.7nits(60nits+10%TP](mailto:9.5%25@66.7nits(60nits+10%25TP) loss) |
| 73 | PWM %[7:0] @ Step 10 | FF | 100%@700nits |
| 74 | Nits [7:0] @ Step 0 | 0F | 15nits |
| 75 | Nits [7:0] @ Step 5 | 3C | 60nits |
| 76 | Nits [7:0] @ Step 10 | 3B | 630nits(700nits-10%TP loss) |
| 77 | Panel Electronics Power @32\*32 Chess Pattern= | 2A | 1.71W |
| 78 | Backlight Power @60 nits= | 0B | 0.45W |
| 79 | Backlight Power @Step 10= | 39 | 4.57W |
| 7A | Nits [7:0] @ 100% PWM Duty= | 3B | 630nits(700nits-10%TP loss) |
| 7B | Nits [15:8] @ Step 10 | 01 | 630nits(700nits-10%TP loss)[15:8] |
| 7C | Nits [15:8] @ 100% PWM Duty= | 01 | 630nits(700nits-10%TP loss)[15:8] |

|  |  |  |  |
| --- | --- | --- | --- |
| **Address** | **Field Name and Comments** | **M125NVF6 R0** | |
| **(Hex)** | **Simulation** | **Note(12.5")** |
| **700nits Ver.** |
| 5B | Flag | 00 |  |
| 5C | Reserved | 00 |  |
| 5D | For Brightness Table and Power cosumption v2 2nd Table(Optional - Privacy Mode) | 03 |  |
| 5E | Flag | 00 |  |
| 5F | PWM %[7:0] @ Step 0 | 04 | [1.7%@5.6nits(5nits+10%TP](mailto:1.7%25@5.6nits(5nits+10%25TP) loss) |
| 60 | PWM %[7:0] @ Step 5 | 33 | [20.2%@66.7nits](mailto:20.2%25@66.7nits) (60nits+10%TP loss) |
| 61 | PWM %[7:0] @ Step 10 | FF | 100%@330nits |
| 62 | Nits [7:0] @ Step 0 | 05 | 5nits |
| 63 | Nits [7:0] @ Step 5 | 3C | 60nits |
| 64 | Nits [7:0] @ Step 10 | 94 | 297nits(330nits-10%TP loss) |
| 65 | Panel Electronics Power @32\*32 Chess Pattern= | 28 | 1.63W |
| 66 | Backlight Power @60 nits= | 12 | 0.72W |
| 67 | Backlight Power @Step 10= | 30 | 3.85W |
| 68 | Nits [7:0] @ 100% PWM Duty= | 94 | 297nits(330nits-10%TP loss) |
| 69 | Nits [15:8] @ Step 10 | 00 | 297nits(330nits-10%TP loss)[15:8] |
| 6A | Nits [15:8] @ 100% PWM Duty= | 00 | 297nits(330nits-10%TP loss)[15:8] |
| 6B | Flags | 00 |  |
| 6C | Detailed Timing Description #4 | 00 |  |
| 6D | Flag | 00 |  |
| 6E | Reserved | 00 |  |
| 6F | For Brightness Table and Power cosumption v2 Primary Table(Sharing Mode) | 02 |  |
| 70 | Flag | 00 |  |
| 71 | PWM %[7:0] @ Step 0 | 06 | [2.4%@16.7nits(15nits+10%TP](mailto:2.4%25@16.7nits(15nits+10%25TP) loss) |
| 72 | PWM %[7:0] @ Step 5 | 18 | [9.5%@66.7nits(60nits+10%TP](mailto:9.5%25@66.7nits(60nits+10%25TP) loss) |
| 73 | PWM %[7:0] @ Step 10 | FF | 100%@700nits |
| 74 | Nits [7:0] @ Step 0 | 0F | 15nits |
| 75 | Nits [7:0] @ Step 5 | 3C | 60nits |
| 76 | Nits [7:0] @ Step 10 | 3B | 630nits(700nits-10%TP loss) |
| 77 | Panel Electronics Power @32\*32 Chess Pattern= | 28 | 1.6W |
| 78 | Backlight Power @60 nits= | 09 | 0.38W |
| 79 | Backlight Power @Step 10= | 30 | 3.85W |
| 7A | Nits [7:0] @ 100% PWM Duty= | 3B | 630nits(700nits-10%TP loss) |
| 7B | Nits [15:8] @ Step 10 | 01 | 630nits(700nits-10%TP loss)[15:8] |
| 7C | Nits [15:8] @ 100% PWM Duty= | 01 | 630nits(700nits-10%TP loss)[15:8] |